

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

EKNER *et al.*

Appl. No.: 09/788,670

Filed: February 21, 2001

For: **Binary Polynomial Multiplier**

Confirmation No.: 6040

Art Unit: 2193

Examiner: Do, Chat C.

Atty. Docket: 1778.2110000

Third Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying IDS Forms are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. Copies of the listed documents are enclosed.

Applicants have listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

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This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application. Attached is our PTO-2038 Credit Card Payment Form in the amount of \$180.00 in payment of the fee under 37 C.F.R. § 1.17(p).

A concise explanation of the relevance of the non-English language document appears below in accordance with 37 C.F.R. § 1.98(a)(3):

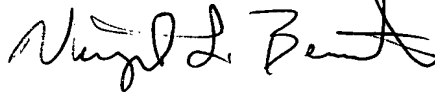
Document FP1 (DE 196 44 688 A1) appears to describe a circuit for digital multiplier assembly for processing binary numbers or Galois Field numbers. An English-language abstract is enclosed as the cover page of document FP1.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

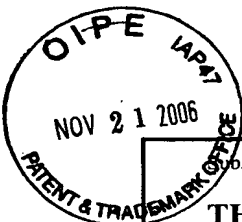


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Date: November 21, 2006

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| THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary) | | | | Complete if Known | |
| | | | | Application Number | 09/788,670 |
| | | | | Filing Date | February 21, 2001 |
| | | | | First Named Inventor | Hartvig W.J. EKNER |
| | | | | Art Unit | 2193 |
| | | | | Examiner Name | Do, Chat C. |
| Sheet | 1 | of | 1 | Attorney Docket Number | 1778.2110000 |

| U.S. PATENT DOCUMENTS | | | | | |
|-----------------------|-----------------------|--|--------------------------------|--|---|
| Examiner Initials* | Cite No. ¹ | Document Number | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
| | | Number-Kind Code ² (if known) | | | |
| | US1 | | | | |
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| FOREIGN PATENT DOCUMENTS | | | | | | |
|--------------------------|-----------------------|---|--------------------------------|--|---|----------------|
| Examiner Initials* | Cite No. ¹ | Foreign Patent Document | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear | T ⁶ |
| | | Country Code ³ Number ⁴ Kind Code ⁵ (if known) | | | | |
| | FP1 | DE 196 44 688 A1 | 04-30-1998 | Technische Universitat Dresden | | |
| | FP2 | | | | | |
| | FP3 | | | | | |
| | FP4 | | | | | |
| | FP5 | | | | | |
| | FP6 | | | | | |
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| | FP9 | | | | | |

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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| | | | | Art Unit | 2193 |
| | | | | Examiner Name | Do, Chat C. |
| Sheet | 1 | of | 1 | Attorney Docket Number | 1778.2110000 |
| NON PATENT LITERATURE DOCUMENTS | | | | | |
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume issue number(s), publisher, city and/or country where published | | | T ² |
| | NPL1 | Drescher, W. and Fettweis, G., "VLSI Architectures for Multiplication in GF(2 ^m) for Application Tailored Digital Signal Processors," in <i>VLSI Signal Processing, IX</i> , San Francisco, California, USA (October 30 - November 1, 1996), IEEE, Piscataway, New Jersey, USA, pp. 55-64. | | | |
| | NPL2 | Drescher, W. <i>et al.</i> , "VLSI Architecture for Datapath Integration of Arithmetic Over GF(2 ^m) on Digital Signal Processors," in <i>IEEE International Conference on Acoustics, Speech, and Signal Processing</i> , Munich, Germany (April 21-24, 1997), IEEE, Los Alamitos, California, USA, pp. 631-634. | | | |
| | NPL3 | Texas Instruments Application Report, "The MSP430 Hardware Multiplier, Functions and Applications," [online] April 1999, [Retrieved on February 16, 2006] Retrieved from the Internet: <URL: http://focus.ti.com/lit/an/slaa042/slaa042.pdf > (34 pages). | | | |
| | NPL4 | INTERSIL Data Sheet, "HS-RTX2010RH: Radiation Hardened Real Time Express Microcontroller," [online] March 2000, [Retrieved on February 16, 2006] Retrieved from the Internet: <URL: http://www.intersil.com/data/fn/fn3961.pdf > (36 pages). | | | |
| | NPL5 | | | | |
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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